REMARKS

After the foregoing amendment, claims 1-24, as amended, are pending in the application. Applicants submit that no new matter has been added to the application by the Amendment.

The Present Invention

The present invention is a packet switch which switches input packets arriving simultaneously at up to M input ports to up to N designated output ports in each of a sequence of frame times by pipelining the input packets through the input module and through a preassigned register to the output port within the frame time of the input packet. In the preferred embodiment, pipelining is accomplished by register selector 134, which determines the availability of a register 106 during the frame time prior to frame of the incoming packet (current frame). Upon arrival of the packet at an input port of the input module in the current frame, the input module routes the packet to the selected register. At a point in the current frame, and possibly before the incoming packet has completely entered the selected register, the output module is set up by the register selector and the contents of the register are pipelined to the output port. Consequently the input packet is transferred to the output port within the current frame time. As made clear in Figs. 2A and 2B, a frame time is the time extent of a packet.

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 1-7, 9, 12-18, 20-22 and 24 as being unpatentable over U.S. Patent No. 4,623,996 (McMillen) in view of U.S. Patent No. 6,931,002 (Simpkens et al.). The Examiner states that McMillen discloses a packet switch having an input module with M inputs and B outputs, a packet buffer including B registers and an output module having B inputs and N outputs. The Examiner also states that McMillen does not teach [switching?] M input packets arriving in each of a sequence of frames times to N output ports, storing the M switches packets into M available registers during each of the frame times to produce M stored packets, and transferring up to N packets from occupied registers to each of the frame times to the output ports based on the destination addresses contained in each of the packets.

The Examiner further states that Simpkens et al. discloses M input packets arriving in each of a sequence of frames times to N output ports, storing the M switched packets into M available registers during each of the frame times to produce M stored packets, and

transferring up to N packets from occupied registers to each of the frame times to the output ports based on the destination addresses contained in each of the packets and it would have been obvious to one of ordinary skill in the art at the time if the invention to modify McMillen to include the features disclosed by Simpkins et al. Applicants respectfully traverse the rejection.

As described at col. 3, lines 1-37, and Figs. 13 and 14, McMillen discloses a packet switching node in which a packet received at one of N input ports is stored during a first frame time in one of M queue buffers by a queue selector, based on a routing tag. The packet is then transferred in a subsequent frame by one of M output arbitrators to one of M output ports designated by the routing tag, in accordance with a predetermined priority arbitration scheme. Accordingly, McMillen requires at least two frame times to move a packet from the input of the queue selector to the output of the arbitrator.

Simpkins et al. discloses a switch for switching both TDM data and packet data. Compared to the prior art the delivery of the TDM data is not delayed or jittered by the presence of packet data.

The switch disclosed by Simpkins et al. comprises input serial to parallel converters, a shared memory, and output parallel to serial converters (Figs. 5 and 6, col. 6, lines 40-59). As described at col. 6, lines 34-39, the [serial] data from each input port must be accumulated until an amount corresponding to the word width of the memory is available before storing the data in the memory. Similarly a word width of parallel data output from the memory must be decomposed into serial data and forwarded out each output in sequence. Consequently, one of ordinary skill in the art would understand that it would take at least two packet (frame) times to transfer an input packet from the switch input to the switch output.

Further, as described at col. 6, lines 10-33, Simpkins et al. discloses that switching is accomplished using the well known technique of time slot interchange (TSI). In time slot interchange, data assigned to a specific input time slot is switched by assigning it to a different time slot. In order to perform this type of switching, the data in each input time slot within a frame must be received before it can be reassigned and output. Again, it requires two frames to transfer a packet at the switch input to the switch output.

Claims 1, 12, 21 and 24 each recite an input module that produces M switched packets, a packet buffer that stores M switched packets and an output module that transfers up to N packets in each frame time.

Applicant respectfully submits that the Examiner is mistaken in stating that the description at col. 3, lines 44-60 and Fig. 5 describes switching an input signal to the output within a single frame. A careful reading of col. 3, lines 44-60 discloses that it is the switching of the packet data has no latency effect on the TDM data. This is consistent with the stated objective of Simpkins et al. and means that the presence of packet data does not delay or jitter the delivery of the TDM data and does not state that there is no latency in the delivery of the TDM data by a consistent one frame time.

Neither McMillen nor Simpkins et al. teach or suggest that the input module produces M switched packets, the packet buffer store M switched packets and the output module transfer up to N packets in each frame time, as recited in claims 1, 12, 21 and 24. Accordingly, the combination of McMillen and Simpkins et al. can not possibly teach all the elements of claims 1, 12, 21 and 24.

Applicants submit that the combination of McMillen and Simpkins et al. does not make claims 1, 12, 21 and 24 obvious. Accordingly Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claim 1, 12, 21 and 24.

In respect to claims 2 and 13, the Examiner states that McMillan discloses an input switch which is an MxN crossbar switch because the McMillan discloses a plurality of input ports 21 and a plurality of output ports. Applicants traverse the rejection.

As understood by those of ordinary skill in the art, a crossbar switch comprises a plurality of vertical paths, a plurality of horizontal paths, and means for interconnecting any one of the vertical paths to any one of the horizontal paths. In other words, any input port of a crossbar switch can be connected to any output port of a crossbar switch.

The Examiner has defined the input module as a combination of the input ports 21 having M inputs and the queue selectors 22 having B outputs (see page 2 of the Office Action). As clearly shown in Fig. 1 of McMillen, an input connected to one port can be connected to only the output of the single queue selector to which that port is connected, and cannot be connected to the output of any other queue selector. Consequently, the input module as defined by the Examiner is not a crosspoint switch. Similarly, the output module has been defined by the Examiner (see page 3 of the Office Action) as a plurality of N output ports 25 and arbitrators 24 having B inputs. As clearly shown, an input to one of the arbitrators 24 can be output on only the single output port connected to that arbitrator and not to the output of any other arbitrator.

Consequently, the output module is not a crossbar switch.

Applicant submits that neither McMillan nor Simpkins et al. teach or suggest an input module and an output module that are crossbar switches, as recited in claims 2 and 13.

Further, it is respectfully submitted that since claims 1, 12, 21 and 24 have been shown to be allowable, claims 2-7, 9, 13-18, 20 and 22 dependent on claims 1, 12 and 21 respectively, are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 2-7, 9, 13-18, 20 and 22.

Allowable Claims

The Examiner objected to claims 8 and 19 as being dependent on a rejected base claim but stated that they would be allowable if rewritten in independent form including the base claim and any intervening claims. Claim 8 depends from allowable claim 1 and claim 19 depends from allowable claim 12. Accordingly, claims 8 and 19 are allowable, at least by their dependency.

Conclusion

Insofar as the Examiner's objections and rejections have been fully addressed, the instant application, including claims 1-24, is in condition for allowance and Notice of Allowability of claims 1-24 is therefore earnestly solicited.

Respectfully submitted,

SHUO-YEN ROBERT LI ET AL.

March 19, 2007
(Date)

By: _____

LOUIS SICKLES II
Registration No. 45,803
AKIN GUMP STRAUSS HAUER & FELD LLP
One Commerce Square
2005 Market Street, Suite 2200
Philadelphia, PA 19103-7013
Telephone: 215-965-1200
Direct Dial: 215-965-1294
Facsimile: 215-965-1210
E-Mail: lsickles@akingump.com

LS: